AMENDMENTS TO THE SPECIFICATION

Please amend the title as follows:

SINGLE DAMASCENE STRUCTURE SEMICONDUCTOR DEVICE HAVING SILICON-DIFFUSED METAL WIRING LAYER ~~AND ITS MANUFACTURING METHOD~~

Page 7, delete the seventh paragraph and insert the following paragraph:

First, referring to Fig. 1A, an insulating underlayer 101 made of silicon dioxide or the like is formed on a silicon substrate (not shown) where various semiconductor elements are formed. Then, an etching stopper 102 made of SiCN is formed by a plasma CVD process on the insulating underlayer~~layer~~ 101. Then, an insulating interlayer 103 made of silicon dioxide is deposited by a CVD process on the etching stopper 102. Then, an anti-reflective coating layer 104 and a photoresist layer 105 are sequentially coated on the insulating interlayer 103. Then, the photoresist layer 105 is patterned by a photolithography process, so that a groove 105a is formed in the photoresist layer 105.

Pages 14-15, delete the bridging paragraph and insert the following paragraph:

First, referring to Fig. 5A, in the same way as in Fig. 1A, an insulating underlayer~~under layer~~ 101 made of silicon dioxide or the like is formed on a silicon substrate (not shown) where various semiconductor elements are formed. Then, an about 50 nm thick etching stopper 102 made of SiCN is formed by a plasma process on the insulating underlayer~~layer~~ 101. Then, an about 400nm thick insulating interlayer 103 made of silicon dioxide is deposited by a plasma CVD process on the etching stopper 102. Then, an anti-reflective coating layer 104 and a

photoresist layer 105 are sequentially coated on the insulating interlayer 103. Then, the photoresist layer 105 is patterned by a photolithography process, so that a groove 105a is formed in the photoresist layer 105. Note that the insulating interlayer 103 can be made of a low-k material having a lower dielectric constant than that of silicon dioxide.